UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/599,396	09/27/2006	Ryosuke Meshii	P30769	8147

7055 7590 12/21/2009

GREENBLUM & BERNSTEIN, P.L.C.
1950 ROLAND CLARKE PLACE
RESTON, VA 20191

EXAMINER	
KUSUMAKAR, KAREN M	
ART UNIT	PAPER NUMBER
2829	

NOTIFICATION DATE	DELIVERY MODE
12/21/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

gbpatent@gbpatent.com
pto@gbpatent.com

Office Action Summary	Application No.	Applicant(s)	
	10/599,396	MESHII ET AL.	
	Examiner	Art Unit	
	KAREN M. KUSUMAKAR	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5,8 and 9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2, 4-5, 8-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 5 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Applicant's admitted prior art*** (herein "AAPA", see pages 1-3 and Figs. 9-10 of instant application) in view of ***Keiichi et al (JP Hei 6-340452, Applicant's admitted prior art)*** and in further view of ***Baret et al. (US 2005/0000561) and Sakurai et al. (US 5,388,460).***

As to claims 1, 5 and 9, AAPA teaches a method for manufacturing a semiconductor physical quantity sensor of electrostatic capacitance type (page 2, line 21-page 3, line 9 and Fig. 9 of the present application) in which mutually facing peripheral areas (referred to as bonding areas) of an insulating substrate and a semiconductor substrate are contacted for anodic bonding (5, Fig. 9 of the present application), while both substrates have an anodic bonding voltage applied therebetween so as to be integrated by anodic bonding (11, Fig. 9 of the present application), with a fixed electrode (7, Fig. 9 of the present application) being formed on a bonding face-side surface of the insulating substrate (2, Fig. 9 of the present application), and with a movable electrode (4, Fig. 9 of the present

application) being formed on a bonding face-side surface of the semiconductor substrate (1, Fig. 9 of the present application), the method comprising: a first step of forming, before the anodic bonding, an equipotential wiring to short-circuit the fixed electrode to the movable electrode on the bonding face-side surface of the insulating substrate/semiconductor substrate inside the bonding area (page 2, lines 21-25 and Fig. 9 of the present application), and to be prevented from being directly sandwiched between the both substrates (Fig. 9 of the present application; 7(7c) connects to substrate 1 indirectly, therefore, indirect sandwiched between the both substrates).

AAPA fails to disclose cutting and removing the equipotential wiring after the anodic bonding in which the equipotential wiring is cut by laser irradiation allowed to pass through from the insulating substrate. However, Keiichi teaches cutting and removing the equipotential wiring after the anodic bonding in which the equipotential wiring is cut by a laser (page 3, lines 19-25 of the present application). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to cut and remove the equipotential wiring after the anodic bonding using a laser as taught by Keiichi in order to make the movable electrode movable and detect a pressure.

AAPA in view of Keiichi does not disclose the equipotential wiring is cut by laser irradiation allowed to pass through from the insulating substrate. However, Baret does teach the cutting of conductors using a laser through a glass substrate (p. 8, [0095]). Therefore, it would have been obvious to one of ordinary

skill in the art at the time the invention was made to cut the equipotential wiring of AAPA in view of Keiichi using the method taught by Baret so as to save on fabrication steps, since the equipotential wiring is under the glass substrate and the glass substrate has the property of allowing the laser irradiation to pass through it.

AAPA does not teach the fixed electrode, the movable electrode, the bonding-face side surfaces of the insulating substrate and the semiconductor substrate, and the equipotential wiring are placed inside the bonding area. However, Sakurai teaches fixed electrode (31), the movable electrode (21), the bonding-face side surfaces of the insulating substrate and the semiconductor substrate (Fig. 1), and the equipotential wiring (32, 41) are placed inside the bonding area (Fig. 1). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to fabricate the electrodes, the bonding surface and the equipotential wiring inside the bonding area so as to use less area on the device, thus reducing cost.

3. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***AAPA*** in view of ***Keiichi***, ***Baret, and Sakurai***, as applied to claims 1 and 5, and further in view of ***Kubo et al. (US 5,977,563).***

As to claims 4 and 8, AAPA in view of Keiichi, Baret, and Sakurai teach conductive film layers (AAPA, 9a and 9b, Fig. 9 of the present application) are exposed at bottom portions of respective through-holes which are provided in the

insulating substrate (AAPA, 8a and 8b, Fig. 9 of the present application) for the fixed electrode (AAPA, 7/7c, Fig. 9 of the present application) and the movable electrode (AAPA, 4, Fig. 9 of the present application) as to cause a current to flow in the equipotential wiring (AAPA, 70, Fig. 9 of the present application).

AAPA in view of Keiichi, Baret, and Sakurai fail to teach the wiring has reduced width at a cutting location thereof. However, Kubo teaches, when cutting a wire with a laser, it is known to form a narrower cutoff portion (col. 6:26-42).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to reduce the width of the cutting location so as to more accurately control the exact cutting location and timing, thus reducing possible damage to other components.

Response to Arguments

4. Applicant's arguments, see amendment filed 9/8/09, with respect to claims 1, 4, 5, 8, and 9 have been fully considered and are persuasive. The previous rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Sakurai and Kubo.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. ***Kato (US 2005/0063125)*** and ***Kawai et al. (US 2001/0045996)*** teach forming a reduced area in a wire where cutting is to be performed.

6. Any response to this Office Action should be faxed to (571) 273-8300 or mailed to:

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Hand-Delivered responses should be brought to:

Customer Service Window

Randolph Building

401 Dulany Street

Alexandria, VA 22313

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KAREN M. KUSUMAKAR whose telephone number is (571) 270-3520. The examiner can normally be reached on Mon - Thurs 7:30a - 5:00p EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/K. M. K./
Examiner, Art Unit 2829
12/12/2009

/Ha T. Nguyen/
Supervisory Patent Examiner, Art Unit 2829